Physics-Based Compact Model of Ferroelectric Semiconductor Field Effect Transistors

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Abstract- The presence of ferroelectric (Fe) and semiconducting properties in two dimensional (2D) In_2Se_3 has made it an interesting material in the field of ferroelectric devices. In particular, Ferroelectric Semiconductor Field Effect Transistors (FeSFET) offer great potential for memory and synaptic applications. In this work, we propose a physics-based compact model of In_2Se_3-based FeSFET. We also present our experimental findings of clockwise (CW) & counter-clockwise (CCW) hysteresis which shows that CW loop is more favorable for high effective oxide thickness (EOT) and thinner In_2Se_3. We show that our calibrated compact model is able to capture these experimental trends with respect to both EOT and In_2Se_3 thickness. The model also provides insights into the physics of CW and CCW hysteretic characteristics of FeSFET, shedding light onto the interplay between polarization switching, semiconductor electrostatics and multi-layer transport in the 2D FeS. Using our model, we analyze FeSFET-based memory array and provide insights into array-driven optimization of EOT and In_2Se_3 thickness to achieve high distinguishability of binary memory states.

I. Introduction

In_2Se_3 is a 2D layered material with both Fe and semiconducting properties [1] and is being explored for the design of various interesting classes of devices [2]. Amongst these, FeS-transistors (FeSFETs) have shown many interesting attributes including the unique presence of both clockwise (CW) and counter-clockwise (CCW) hysteresis [3]. However, the modeling and understanding of its rich characteristics are fairly limited. In [3], 1D models shed some light onto the behavior of FeSFETs, but are not suitable for exploring circuit applications. In this work, we propose a physics-based compact model of In_2Se_3 FeSFET. Our model incorporates the 2D semiconducting properties and ferroelectric attributes simultaneously. Using the proposed model, we establish the conditions for obtaining CW and CCW hysteresis. In particular, we analyze the effect of EOT and FeS thickness on the transfer characteristics of FeSFETs. We also present our experimental data on FeSFETs establishing that the model prediction is in a close match with the experiment. Lastly, we perform memory array analysis using our compact model.

II. The Proposed Compact Model

Fig. 1 shows our modeling framework for the back-gated FeSFET device (Fig. 1(a) - similar to the structure demonstrated in the experiments [3]). We use a capacitive network [4] to model the electrostatic interactions between the back-gate, gate oxide and FeS. Note, we significantly expand on the approach in [4] (which assumes a monolayer) and include two semiconducting surfaces – top and bottom with potentials V_1 and V_2, respectively, as shown in Fig. 1b. The two surfaces represent the dominating current conducting channels, as suggested in [3]. The gate oxide capacitance (C_{ox}) and background dielectric capacitance of semiconductor (C_{2d}) are modeled using linear capacitance. The surface potential of top and bottom surfaces of the FeS material are modeled considering 2D charge density of Q_1 and Q_2. The ferroelectric nature of the FeS material is considered through the Miller (Preisach) model [5], which models the major/minor polarization-voltage (P-V) loops of ferroelectric. The corresponding Miller capacitance is placed between the top and bottom surfaces such that the difference between V_1 and V_2 determines the electric field for the Miller equation. We use different positive and negative coercive fields (E_c) for forward and backward paths as suggested by experimental evidence [6]. An effective screening coefficient (β) at the top surface is considered to capture the charge screening from source/drain contacts as well as fringing field. The capacitive network is self-consistently solved at the source and drain (following the approach in [4]) to obtain the surface potential and charge at the top and bottom surfaces as shown in Figure 1c. These surface potentials are used to obtain the current on the top (I_{top}) and bottom (I_{bot}) surfaces considering both electron and hole components. The deduced layer-wise compact current equations have different forms in different regimes of V_1 and V_2 and are depicted in Fig. 1d. The total current (I_{tot}) is obtained by summing the currents from the two surfaces.

III. Experiments & Model Calibration

The key experimental steps for fabrication of In_2Se_3 FET and device characterization are mentioned in Fig. 2. For simulation, we calibrate the FeSFET with low EOT (15 nm HfO_2) and high EOT (90 nm SiO_2) as in the experiments [3]. The simulated characteristics and corresponding experimental characteristics are shown in Fig. 3. The model captures the drain current variation with gate voltage for both devices. As shown in the experiment with 5V sweep, CCW hysteresis of drain current is observed in low EOT device. On the other hand, with 40V sweep, CW hysteresis of drain current is observed in high EOT device. The two devices have identical structures except for the back gate oxide material, its thickness and FeS thickness. Note that the memory window (MW) from simulation does not exactly match with experiment. This is possibly due to interface trap charges, variability, etc.

IV. Analysis of Hysteresis Loops

A. Low EOT Device

To explain how our model captures the hysteretic characteristics of FeSFET, let us first look at the polarization with respect to gate voltage in Fig. 4a for low EOT device. Initialization cycle is considered by applying a negative voltage and thus obtaining negative polarization. Now, when

we apply a sufficiently positive gate voltage (V_{GS}) sweep, it switches P to a positive value in the forward path. In the reverse path, P reverses to a negative value. The polarization follows the Preisach model as described earlier (see Fig. 4b). Note that the flat region during switching around P=0 in Fig. 4a mainly originates due to the depletion of mobile carriers at the top and bottom surfaces. At that condition, both top and bottom surface responds to the gate voltage at a similar rate and Fe capacitor voltage remains fixed.

In the reverse path, due to the hysteretic nature of ferroelectric, higher polarization magnitude persists compared to forward path. This induces higher positive (negative) bound charges at the top (bottom) surface in the backward path compared to the forward path. The positive (negative) bound charges at the top (bottom) surface increase (reduce) its potential. Thus, the bottom surface potential exhibits CW hysteresis loop, while for the top surface, CCW hysteresis is observed (Fig. 5). The mobile charges at the top and bottom surfaces are defined by the corresponding surface potentials. As a result, the bottom and top surface currents show CW and CCW hysteresis, respectively, as shown in Fig. 6.

The total current mainly follows the larger of the top and bottom currents. Here, two effects come into picture: (1) the polarization magnitude and (2) the coupling of the top layer to gate bias. During the forward path, the initial negative polarization in FeS during the forward path leads to positive (negative) bound charges on the bottom (top) surface, thus reducing (increasing) the threshold voltage. Also, electron concentration in the top layer is lower than the bottom layer due to weaker gate coupling. Therefore, bottom current dominates. During the backward path, the polarization reversal results in negative (positive) bound charges on the bottom (top) surfaces. Also, top surface responds less to gate voltage and shows larger electron concentration than bottom surface at negative voltages. Because of these two effects, the top layer backward electron current surpasses the bottom layer forward current at a particular voltage. As in our region of interest electron current is dominant, the total current shows a CCW loop, as indicated in Fig. 6.

Next, we vary the maximum sweep voltage magnitude ($V_{max,sweep}$) and calculate the hysteresis loop. Fig. 7 shows that the MW increases with increasing $V_{max,sweep}$ and saturates. This happens due to the polarization saturation. We also present the output characteristics in Fig. 8 showing excellent match of the maximum ON current with experiment [3].

B. High EOT Device

To understand the origin of the CW loop in the high EOT device, we plot the polarization with respect to gate voltage. Fig. 9 shows that from the initial negative polarization, the device starts switching the polarization with increasing voltage but due to the high EOT (less potential across FeS), the polarization cannot reverse. The corresponding P vs capacitor voltage in the inset of Fig. 9 shows the minor loop trajectory. As described before and denoted by the polarization bound charges in Fig. 9, the backward path of bottom (top) surface has less positive (negative) bound charge compared to forward path. Therefore, similar to the P reversal in low EOT device, the bottom and top surface potential shows CW and CCW loop, respectively (Fig. 10). However, for high EOT, in both forward and backward path, the top surface electron current is extremely low. This is because the bound charges at the top surface are always negative in this case, thus reducing mobile electrons at the top surface. The overall current is dominated by the bottom layer current, which, in effect, leads to CW hysteretic characteristics for the overall current.

Next, we vary $V_{max,sweep}$ and calculate the hysteresis loop (Fig. 11). Due to less polarization switching, MW reduces with reducing $V_{max,sweep}$ which is in agreement with experiments [7].

V. FeS Thickness Scaling

Coercive field of ferroelectric materials is widely known to increase with thickness scaling. For In_2Se_3, several experiments have reported a similar trend [6][8]. Following [6], we use an inverse relation of E_c and FeS thickness (for 15 nm HfO_2 gate insulator) as shown in Fig. 12. We present both experimental and simulation hysteresis loops in Fig.13. As can be seen, our compact model captures the experimental hysteretic characteristics well. As we thin down In_2Se_3 from 96 nm to 14.7 nm, the CCW loop reduces (Fig. 13a-b). This is because although effective electric field in the FeS increases with thinner In_2Se_3, the effect of increase in E_c is much more. Therefore, the polarization reversal becomes more difficult with thinner FeS and MW of CCW loop reduces. If we reduce FeS thickness further (to 5.6 nm), E_c increases to such a large extent that P cannot reverse at 5V and we obtain CW loop (Fig. 13(c). Thus, FeS thickness turns out to be a crucial parameter for the desired characteristics of CW or CCW hysteresis loop.

VI. Memory Performance analysis

Let us now analyze the memory performance of FeSFET using our compact model. First, we use our compact model to find suitable design point for a scaled FeSFET memory device (see Fig. 14), based on which we design a 64x64 array. The parameters and read/write pulses are shown in Fig. 14. We first initialize all the FeSFETs to -5 V and perform a global set to write LRS. Then we reset the targeted cells for selectively writing HRS. The bit cell performance parameters are shown in Fig. 15 for 5.6 nm and 14.7 nm FeS thickness. The LRS to HRS current ratio shows excellent distinguishability and increases for lower FeS thickness. Using the bit cell level analysis, we calculate the worst case LRS to HRS ratio for the full memory array (i.e. considering leakage in the unaccessed cells) for different thicknesses of In_2Se_3 and HfO_2 as shown in Fig. 16. Our analysis suggests that within the considered range, scaling of gate oxide and FeS thickness enhances LRS to HRS distinguishability and provides better memory performance.

VII. Conclusion

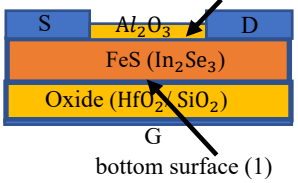
In summary, we propose a physics-based compact model for ferroelectric semiconductor FET. The calibrated model not only captures experimental trends of clockwise (CW) and counterclockwise (CCW) hysteresis loop for high EOT, low EOT and scaled FeS thickness but also provides a physics-based understanding of these unique characteristics. Based on our model, we analyze FeSFET based memory array and provide circuit-driven FeSFET design insights.

Acknowledgement: This work was supported by NSF.

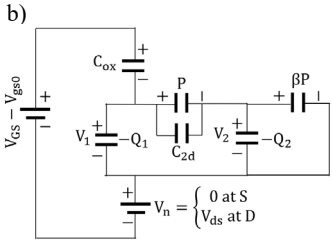
References: [1] *Nat Commun* **8**, 14956 (2017) [2] *Nat Commun* **12**, 53 (2021) [3] *Nat Electron* **2**, 580 (2019) [4] *Appl. Phys. Lett.* 101, 243501 (2012) [5] *J. Appl. Phys.* 68, 6463–6471 (1990) [6] *J. Appl. Phys. 132, 054101 (2022) [7]* ACS Nano *2023, 17, 6095−6102 [8] Nano Res. 13, 1897–1902 (2020)*

2D Ferroelectric Semiconductor (FeS) FET: Compact Model

a)



b)



c)

Self-consistent module

Ferroelectric equations (Preisach Model):

$$V_{cap} = (V_1 - V_2)\big|_{\text{averaged for S and D}}$$

Major Loop:

$$P = P_{sat} = \begin{cases} P_s \tanh\left[\dfrac{V_{cap} - V_{cp}}{2\delta}\right]; \text{if } dV_{cap} > 0 \\ P_s \tanh\left[\dfrac{V_{cap} + V_{cn}}{2\delta}\right]; \text{if } dV_{cap} < 0 \end{cases}$$

where, $\delta = \dfrac{V_{cp} + V_{cn}}{2} \dfrac{1}{\ln\left(\frac{1 + P_r/P_s}{1 - P_r/P_s}\right)}$

Minor Loop: $\dfrac{\delta P}{\delta V} = \Gamma \dfrac{\delta P_{sat}}{\delta V}$

where, $\Gamma = 1 - \tanh[(\dfrac{P - P_{sat}}{\pm P_s - P})^{1/2}]$

Semiconductor 2D Charge Equations:

$$Q_{i,elec} = -q \times N_{2D} \ln\left(1 + e^{\frac{qV_i - E_0}{kT}}\right); N_{2D} = \frac{m_e kT}{\pi\hbar^2}$$

$$Q_{i,hole} = q \times N_{2Dp} \ln\left(1 + e^{\frac{-qV_i - (E_g - E_0)}{kT}}\right); N_{2Dp} = \frac{m_h kT}{\pi\hbar^2}$$

$$Q_i = Q_{i,elec} + Q_{i,hole}; i = 1,2;$$

E_0 & V_i are CB and fermi level w.r.t. midgap

Q_1, Q_2 ↓ ↑ V_1, V_2

P →

V_1 ←

V_2 ←

Charge Neutrality Equations:

(1) $(V_{GS} - V_1 - V_{gs0} - V_n)C_{ox} = -Q_1 + (V_1 - V_2)C_{de} + P$

(2) $(V_1 - V_2)C_{de} + (1 - \beta)P = -Q_2$

β is effective screening coefficient at top layer

V_1, V_2 at S & D ($V_{1,s}$, $V_{1,d}$, $V_{2,s}$, $V_{2,d}$) ↓

d)

Electron current equations: $I_{tot} = I_{bot} + I_{top}$

$$I_{bot} = -\mu_n \frac{W}{L} \int_0^{V_{ds}} Q_1 dV_n = -\mu_n \frac{W}{L} [(g_{11,d} - g_{11,s}) + \frac{1}{C_{ox}}(g_{12,d} - g_{12,s}) + \frac{1}{C_{ox}}(g_{13,d} - g_{13,s})]$$

$$I_{top} = -\mu_n \frac{W}{L} \int_0^{V_{ds}} Q_2 dV_n = -\mu_n \frac{W}{L} [(g_{21,d} - g_{21,s}) + \left\{\frac{1}{C_{ox}} + \frac{1}{C_{de}}\right\}(g_{22,d} - g_{22,s}) + \frac{1}{C_{ox}}(g_{23,d} - g_{23,s})]$$

$$g_{i1,j} = \begin{cases} kTN_{2D} e^{\frac{qV_{i,j} - E_0}{kT}} \text{ for } qV_{i,j} < E_0 \\ q^2 D_0 \frac{V_{i,j}^2}{2} - qD_0(E_0 - kT)V_{i,j} \text{ for } qV_{i,j} \geq E_0 \end{cases}$$

$$g_{i2,j} = \frac{Q_{i,j}^2}{2} \qquad D_0 = \frac{N_{2D}}{kT} \qquad (i = 1,2 \ \& j = s,d)$$

For $qV_{1,j} < E_0, qV_{2,j} < E_0$: $g_{13,j} = e^{-a(Q_{2,j}+P)} \frac{(aQ_{2,j}+1)}{a^2}$; $g_{23,j} = e^{-a(Q_{2,j}+P)} \frac{-a^2 Q_{2,j}^2 - aQ_{2,j} - 1}{a^2}$; $a = \frac{q}{kTC_{de}}$

For $qV_{1,j} \geq E_0, qV_{2,j} \geq E_0$: $g_{13,j} = \left(1 + \frac{q^2 D_0}{C_{de}}\right) \frac{Q_{2,j}^2}{2} + \frac{q^2 D_0 P}{C_{de}} Q_{2,j}$; $g_{23,j} = \left(1 + \frac{q^2 D_0}{C_{de}}\right) \frac{Q_{2,j}^2}{2}$

For $qV_{1,j} \geq E_0, qV_{2,j} < E_0$: $g_{13,j} = q^2 D_0 N_{2D} e^{\frac{qV_{2,j} - E_0}{kT}} \left[\frac{q^2 N_{2D}}{2C_{de}} e^{\frac{qV_{2,j} - E_0}{kT}} + qV_{2,j} - \left(E_0 + \frac{qP}{C_{de}}\right)\right]$; $g_{23,j} = q^3 D_0 N_{2D} \left[\frac{qN_{2D}}{2C_{de}} e^{\frac{2(qV_{2,j} - E_0)}{kT}} + \frac{kT}{q} e^{\frac{qV_{2,j} - E_0}{kT}}\right]$

For $qV_{1,j} < E_0, qV_{2,j} \geq E_0$: $g_{13,j} = \frac{q^2 N_{2D}^2}{\left(1 + \frac{q^2 D_0}{C_{de}}\right)} e^{\frac{qV_{1,j} - E_0}{kT}}$; $g_{23,j} = q^2 D_0 e^{\frac{qV_{1,j} - E_0}{kT}} [\frac{q^2 D_0}{\left(1 + \frac{q^2 D_0}{C_{de}}\right)} \{\left(\frac{kT}{q}\right)^2 \left(\frac{qV_{1,j}}{kT} - 1\right) + \frac{kT}{q} \cdot \frac{qD_0(E_0 - kT) + P}{C_{de}}\} - D_0 kT(E_0 - kT)]$

Hole current is obtained by replacing μ_n by μ_p, E_0 by $(E_g - E_0)$, adding negative sign before q and inverting the inequalities.

Fig. 1 In_2Se_3-based FeSFET a) device structure b) equivalent circuit c) self-consistent module and d) current equations. Parameters: $m_{e/h} = 0.1m_0$, $V_{gs0} = -1.8$ V, $E_g = 1.4$ eV, $E_0 = 0.7$ eV, $L = 1$ μm $\mu_n = 45$ cm^2/Vs, $\mu_p = 10^{-4}$ cm^2/Vs, $P_s = 3$ μC/cm^2, $P_r = 2.5$ μC/cm^2, $\varepsilon_{r2d} = 1.5$, $\varepsilon_{r,HfO_2} = 30$, $\varepsilon_{r,SiO_2} = 3.9$, $\beta = 0.3$

Calibration of compact model with experiments

Experimental steps:

- Oxide deposition on p+ Si
- α- In_2Se_3 transfer on oxide with scotch tape exfoliation
- Ti/ Au deposited by electron-beam evaporation and liftoff
- ALD of Al_2O_3 capping layer
- AFM, SEM, EDS for characterization
- DC electrical measurement in dark and at room temperature

Fig. 2 Key experimental steps for device fabrication and measurement [3]

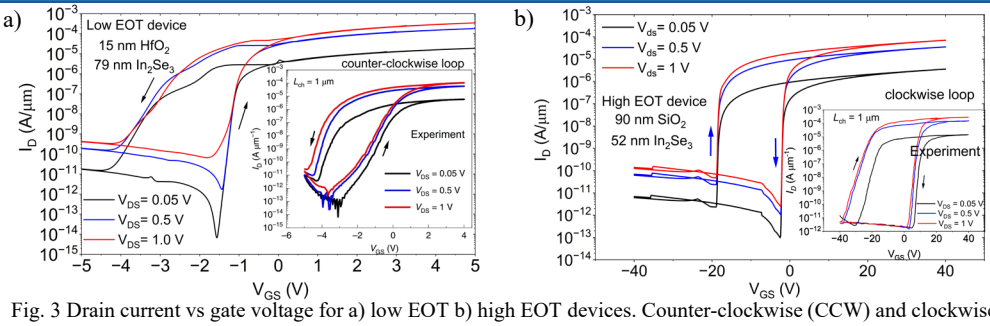


Fig. 3 Drain current vs gate voltage for a) low EOT b) high EOT devices. Counter-clockwise (CCW) and clockwise (CW) loops are obtained for a) and b), respectively. Compact model captures the experimental trends [3].

Switching mechanisms for clockwise and counterclockwise hysteresis: EOT and FeS thickness dependence

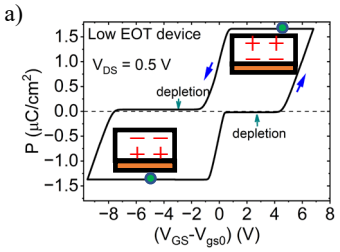
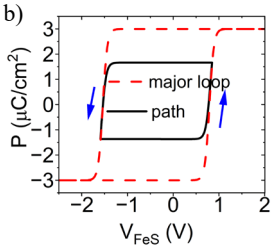


Fig. 4 a) Polarization (P) vs gate voltage b) P vs potential across FeS. The flat region around zero P arises due to carrier depletion, which leads to top and bottom potential changing with the same slope w.r.t. V_{GS} yielding ~zero change in V_{FeS}. $E_{cn} = 0.02$ V/nm & $E_{cp} = 0.01$ V/nm for low EOT.



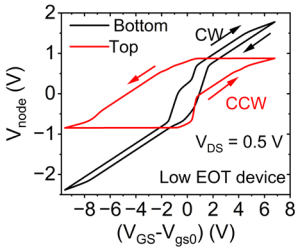


Fig. 5 Potential at top and bottom surfaces of FeS. P switching yields top and bottom surface potential to be CCW and CW, respectively.

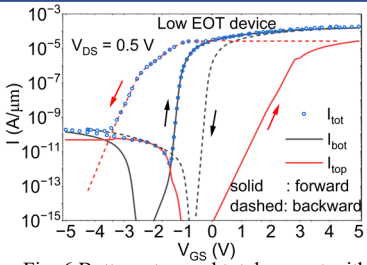


Fig. 6 Bottom, top and total current with V_{GS}. I_{tot} follows the dominant layer in forward and backward path (CCW overall).

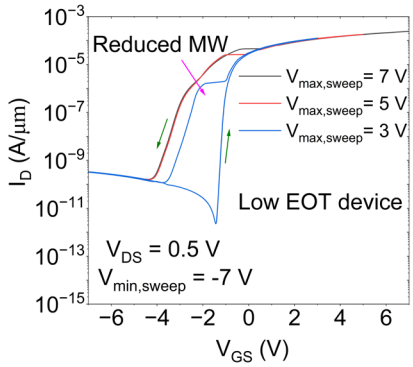


Fig. 7 Drain current with varying positive sweep voltage. With reduction in V_{sweep}, MW reduces

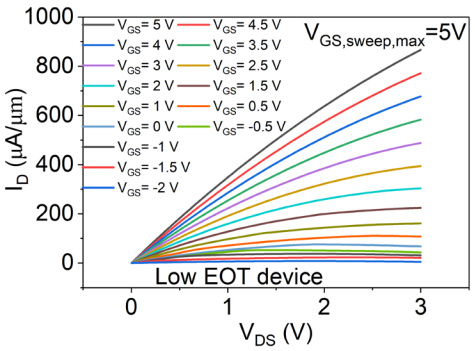


Fig. 8 I_D variation with V_{DS}. The maximum on current is 866 μA/μm that matches well with experiments [3].

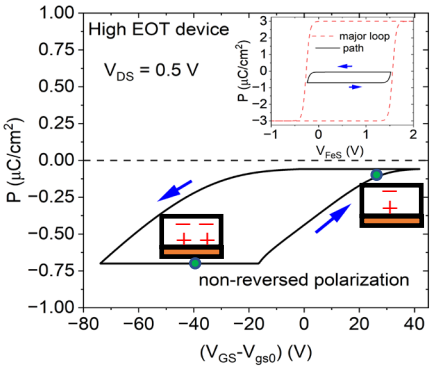


Fig. 9 P vs gate voltage for high EOT device. Polarization does not reverse. Inset shows the P vs FeS voltage. E_{cn} = 0.005 V/nm & E_{cp} = 0.03 V/nm.

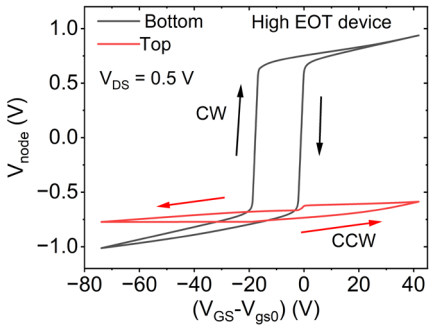


Fig. 10 Potential at top (CCW) and bottom surfaces (CW). Top layer current remains negligible due to non-reversal of P. I_{tot} follows I_{bot} to become CW.

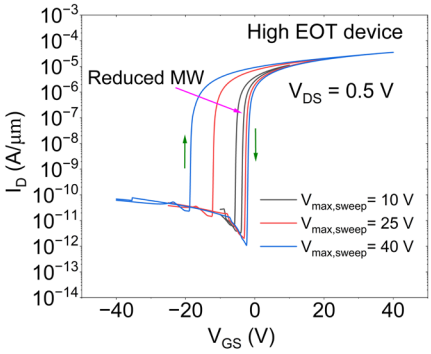


Fig. 11 I_D with reduced sweep voltage magnitude. MW reduces as in experiment [7].

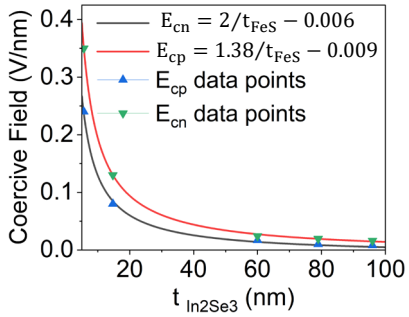


Fig. 12 Coercive field asymmetry & variation with In_2Se_3 thickness for HfO_2 gate dielectric. Asymmetry & inverse relation are used as in experiments [6][8].

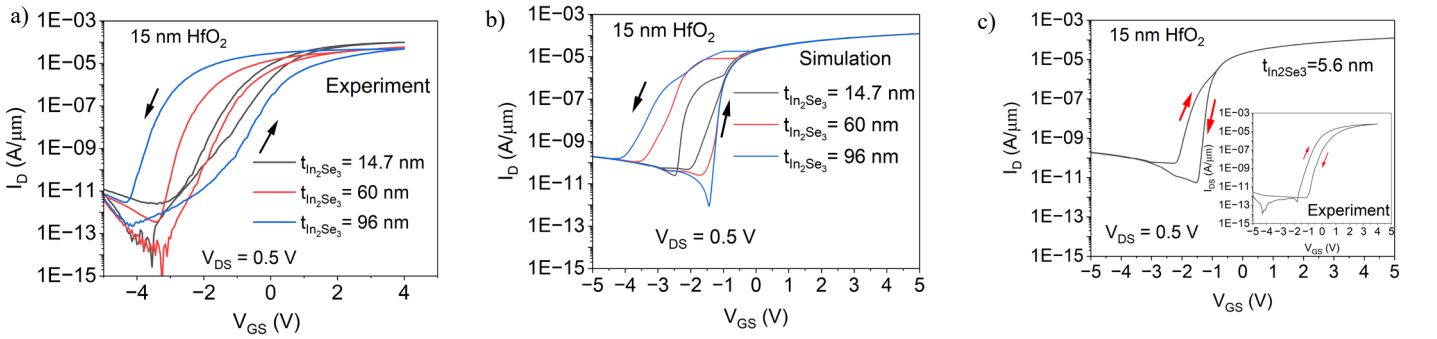
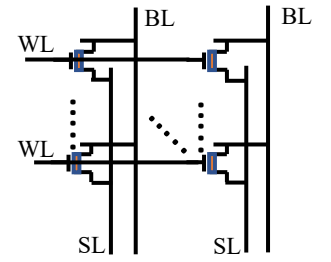


Fig. 13 Effect of reduced FeS thickness a) Experimental data showing reduction of CCW hysteresis b)Simulation results from our compact model c) CW hysteresis at ultra-thin FeS samples. With scaling down, increase in coercive field hinders polarization reversal and leads to CW loop.

Bit cell and array level simulation



64×64 bit FeSFET memory array

t_{ox}	1.5 nm	L	30 nm
W	50 nm	V_{gs0}	1.7 V

Global V_{set}	5 V
Selective V_{reset}	-3.3 V
$V_{unaccessed}$	$\pm V_{set}/3$
$V_{GS,read}$	1.2 V
$V_{DS,read}$	0.5 V

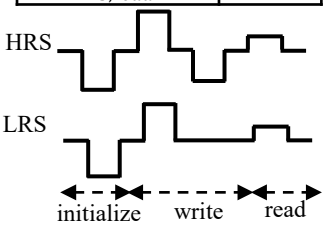


Fig. 14 FeSFET based memory array and read-write operation. Standard $V_{set}/3$ inhibition bias scheme is used for write operation.

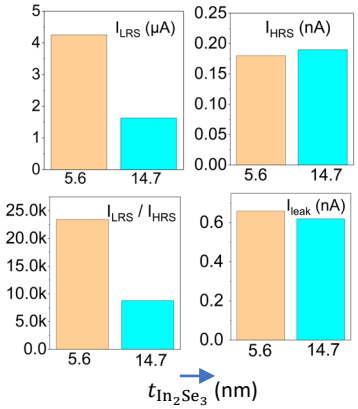


Fig. 15 Bit cell-level memory performance for different In_2Se_3 thicknesses with the proposed model

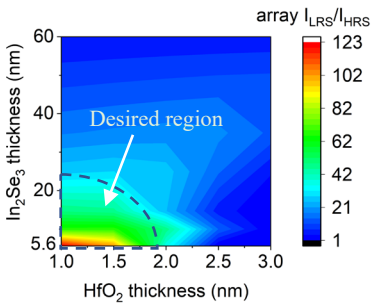


Fig. 16 Array-level worst case ratio of LRS to HRS currents. Scaling of gate oxide and FeS thickness enhance distinguishability.